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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/026,618	12/27/2001	Seung-Hwan Lee	P67474US0	9115

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EXAMINER
BAYARD, EMMANUEL

ART UNIT	PAPER NUMBER
2638	

DATE MAILED: 07/12/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/026,618	LEE ET AL.	
	Examiner	Art Unit	
	Emmanuel Bayard	2638	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *27 December 2001*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-8* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-8* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *12/27/01*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

2. Claims 1-8 are rejected under 35 U.S.C. 102(e) as being anticipated by Hiramatsu et al U.S. Patent No 6,456,677 B1.

As per claims 1, 5 Hiramatsu teaches a synchronization system in digital communication, comprising: an "A/D" converter is the same as the claimed (converter for receiving signals from a transmitter, and over-sampling a single symbol interval into a plurality of sub-samples (see figs.2, 9-10, 16, 27-33 elements, 14, 804, 808, 1004, 1603, 1604); a signal processor for classifying each symbol over-sampled by the converter into a sub-sample group according to a sample phase (see fig.29 and col.35, lines 35-49), and performing signal processing to adjust processing speeds (see col.24, lines 8-20); an integrator (see fig.29 element 2601 and col.8, lines 63-67) for removing noise from the signals output by the signal processor and performing integration during a predetermined time; and a timing selector for selecting an optimal symbol synchronization point from among values output by the integrator, generating a symbol timing signal and outputting it (see fig.13 element 1314 and col.2, lines 60-62 and col.5,

lines 13-15 and col.14, lines 35-60 andcol.20, lines 40-60 and col.33, lines 23-29).

As per claim 2, Hiramatsu teaches, further comprising a digital demodulator (see figs.2, 9 elements 16, 806) for receiving the symbol-timing signal from the signal processor and the timing selector, generating a demodulation signal, and outputting it.

As per claim 3, Hiramatsu teaches wherein the signal processor comprises: a sample arranger for classifying the over-sampled signal output by the converter into a sub-sample group according to a sample phase within the symbol (see fig.29 and col.35, lines 35-49),; and an absolute value calculator (see fig.16 element 1606-1607) for converting the sub-sample values output by the sample arranger into absolute values.

As per claim 4 Hiramatsu teaches, wherein the signal processor comprises: a sample arranger for classifying the over-sampled signal output by the converter into a sub-sample group according to a sample phase within the symbol (see fig.29 and col.35, lines 35-49); and a sign selector for selecting signals having only either sign from among the respective sub-sample values having positive and negative signs (see col.40, lines 40-60), the sub-sample values being output by the sample arranger.

As per claim 6, Hiramatsu teaches, wherein (c) comprises selecting the optimal symbol synchronization point (see col.2, lines 60-62 and col.5, lines 13-15 and col.14, lines 35-60 andcol.20, lines 40-60 and col.33, lines 23-29, and generating a digital demodulation signal(see figs.2, 9 elements 16, 806) using the selected signal and outputting it.

As per claim 7, Hiramatsu teaches, wherein the signal processing in (b) converts

sub-sample values that are output after they are classified into the sub-sample group into absolute values (see fig.27 element 1606, 1607).

As per claim 8, Hiramatsu teaches, wherein the signal processing in (b) selects signals having an either sign from among sub-sample values having positive and negative signs (see col.40, lines 40-60), sub-sample values being output after being classified into the sub-sample group.

Conclusion

3. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Yasuda et al U.S. Patent No 4578,800 teaches a synchronization circuit.

Yokozawa et al U.S. Patent No 6,570,622 B2 teaches a magnetic card.

Aono et al U.S. Patent No 5,844,950 teaches a cross polarization interference.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Emmanuel Bayard whose telephone number is 571 272 3016. The examiner can normally be reached on Monday-Friday (7:Am-4:30PM) Alternate Friday off.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Vanderpuye Kenneth can be reached on 571 272 3078. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Emmanuel Bayard
Primary Examiner
Art Unit 2638

7/5/05

EMMANUEL BAYARD
PRIMARY EXAMINER